LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended)

A control circuit for controlling a driving circuit for driving a power device, comprising:

sensing circuitry for providing a sense result signal for controlling said driving circuit in response to a sense input signal, the sense input signal including information received from the power device <u>over a direct circuit path from said power device to said sensing circuitry</u>; the sense result signal including information derived from the sense input signal about operation of the power device; and

correction circuitry <u>included in said direct path from said power device to said sensing circuitry</u> for preventing the sense input signal <u>on said circuit path</u> from including spurious information received from the power device.

Claim 2 (Previously Presented)

The circuit of claim 1 in which the information from the power device includes spurious negative spikes, the correction circuitry preventing negative spikes in the sense input signal.

Claim 3 (Previously Presented)

The circuit of claim 2, further comprising a gating device connected between the sensing circuitry and the power device, in which the gating device is a diode and the power device is a field effect transistor (FET); the diode being turned on when the FET is on and being turned off when the FET is off; the correction circuitry preventing negative spikes in the sense input signal except when the FET is on.

Claim 4 (Original)

The circuit of claim 1 in which the sensing circuitry includes a comparator for comparing signals received at first and second inputs and for providing the sense result signal at an output,

the first input receiving the sense input signal and the second input receiving a reference signal; the correction circuitry receiving the sense results signal from the comparator's output and preventing negative spikes in the sense input signal when the sense result signal indicates that the sense input signal is greater than the reference signal.

Claim 5 (Previously Presented)

The circuit of claim 4, further comprising an integrated circuit that includes the sensing circuitry and the correction circuitry; the integrated circuit further including:

a sensing node for connecting to the power device; and

a voltage source connected to provide the reference signal to the comparator's second input, a first resistance between a supply voltage and the sensing node, a second resistance between the sensing node and the comparator's first input, and a third resistance between the comparator's first input and ground; the voltage source and the first, second, and third resistances having values such that the sense input signal drops below the reference signal if the gating device turns on; the correction circuitry including a switchable impedance parallel to the first resistance, the switchable impedance being turned on only when the sense result signal indicates that the sense input signal is greater than the reference signal.

Claim 6 (Previously Presented)

The circuit of claim 1, further comprising an integrated circuit that includes the sensing circuitry and the correction circuitry; the integrated circuit further including a sensing node for connecting to the power device; the correction circuitry including a switchable impedance between a power supply and the sensing node and switching circuitry for switching the impedance on and off in response to a device state signal indicating whether the power device is on or off, the switchable impedance being turned on except when the device state signal indicates that the power device is on.

Claim 7 (Original)

The circuit of claim 6 in which the correction circuitry further includes a comparator for comparing signals received at first and second inputs and for providing the device state signal at its output, the first input receiving a voltage at the sensing node and the second input receiving a reference voltage; the comparator's output being connected for turning the switchable impedance on only when the device state signal indicates that the sensing node voltage is greater than the reference voltage.

Claim 8 (Original)

The circuit of claim 6 in which the sensing circuitry provides the device state signal to the switching circuitry.

Claim 9 (Currently Amended)

An integrated control circuit for controlling a driving circuit for driving a power device, comprising:

a sensing node for connecting to the power device;

sensing circuitry for providing a sense result signal for controlling said driving circuit in response to a sense input signal, the sense input signal including information received at the sensing node from the power device <u>over a direct circuit path from said power device to said sensing circuitry</u>; the sense result signal including information derived from the sense input signal about operation of the power device; and

correction circuitry <u>included in said direct circuit path from said power device to said sensing circuitry</u> for preventing the sense input signal <u>on said circuit path</u> from including spurious information received at the sensing node from the power device.

Claim 10 (Previously Presented)

The circuit of claim 9 in which the sensing node is a desat/voltage feedback pin and in which the information from the power device includes spurious negative spikes to the sensing

node, the correction circuitry being connected to the sensing node to prevent negative spikes in the sense input signal.

Claim 11 (Previously Presented)

The circuit of claim 10, further comprising a gating device connected between the sensing circuitry and the power device, in which the gating device is a diode and the power device is a field effect transistor (FET); the diode being turned on when the FET is on and being turned off when the FET is off; the correction circuitry preventing negative spikes in the sense input signal except when the FET is on.

Claim 12 (Original)

The circuit of claim 9 in which the sensing circuitry includes a comparator for comparing signals received at first and second inputs and for providing the sense result signal at an output, the first input receiving the sense input signal and the second input receiving a reference signal; the correction circuitry receiving the sense result signal from the comparator's output and preventing negative spikes in the sense input signal only when the sense result signal indicates that the sense input signal is greater than the reference signal.

Claim 13 (Original)

The circuit of claim 12, further comprising a voltage source connected to provide the reference signal to the comparator's second input, a first resistance between a supply voltage and the sensing node, a second resistance between the sensing node and the comparator's first input, and a third resistance between the comparator's first input and ground; the capacitance and the first, second, and third resistances having values such that the sense input signal drops below the reference signal if the gating device turns on; the correction circuitry including a switchable impedance path parallel to the first resistance, the switchable impedance path being turned on only when the sense result signal indicates that the sense input signal is greater than the reference signal.

Claim 14 (Original)

The circuit of claim 9 in which the correction circuitry includes a switchable impedance between a power supply and the sensing node and switching circuitry for switching the impedance on and off in response to a device state signal indicating whether the power device is on or off, the switchable impedance being turned on except when the device state signal indicates that the power device is on.

Claim 15 (Original)

The circuit of claim 14 in which the correction circuitry further includes a comparator for comparing signals received at first and second inputs and for providing the device state signal at its output, the first input receiving a voltage at the sensing node and the second input receiving a reference voltage; the comparison result signal being connected for turning the switchable impedance on only when the device state signal indicates that the sensing node voltage is greater than the reference voltage.

Claim 16 (Original)

The circuit of claim 14 in which the sensing circuitry provides the device state signal to the switching circuitry.

Claim 17 (Currently Amended)

An integrated control circuit for controlling respective high side and low side driving circuits for driving high and low side power devices connected in a half bridge, the control circuit comprising high side circuitry for controlling the high side driving circuit and low side circuitry for controlling the low side driving circuit;

the high side circuitry comprising:

a first sensing node for connecting to the high side power device;

first sensing circuitry for providing a first sense result signal for controlling said high side driving circuit in response to a first sense input signal, the first sense input signal including information received at the first sensing node from the high side power device <u>over a first direct</u>

circuit path from said high side power device to said first sensing circuitry; the first sense result signal including information derived from the first sense input signal about operation of the high side power device; and

first correction circuitry included in said first direct circuit path from said high side power device to said first sensing circuitry for preventing the first sense input signal on said first circuit path from including spurious information received at the first sensing node; and

the low side circuitry comprising:

a second sensing node for connecting to the low side power device;

second sensing circuitry for providing a second sense result signal for controlling said low side driving circuit in response to a second sense input signal, the second sense input signal including information received at the second sensing node from the low side power device over a second direct circuit path from said low side power device to said second sensing circuitry; the second sense result signal including information derived from the second sense input signal about operation of the low side power device; and

second correction circuitry included in said second direct circuit path from said low side power device to said second sensing circuitry for preventing the second sense input signal on said second circuit path from including spurious information received at the second sensing node.

Claim 18 (Previously Presented)

The circuit of claim 1, further comprising a driving circuit, wherein said driving circuit receives an input voltage and generates a driving signal for said power device.

Claim 19 (Previously Presented)

The circuit of claim 9, further comprising a driving circuit in said integrated circuit, wherein said driving circuit receives an input voltage and generates a driving signal for said power device.

Claim 20 (Currently Amended)

An integrated control circuit for controlling respective high side and low side driving circuits for driving high and low side power devices connected in a half bridge, the integrated control circuit comprising high side circuitry for controlling the high side driving circuit and low side circuitry for controlling the low side driving circuit;

the high side circuitry comprising:

a first sensing node for connecting to the high side power device;

first sensing circuitry for providing a first sense result signal for controlling said high side driving circuit in response to a first sense input signal, the first sense input signal including information received at the first sensing node from the high side power device <u>over a first direct circuit path from said high side power device to said first sensing circuitry</u>; the first sense result signal including information derived from the first sense input signal about operation of the high side power device; and

first correction circuitry <u>included in said first direct circuit path from said high side power device to said first sensing circuitry</u> for preventing the first sense input signal <u>on said first circuit path</u> from including spurious information received at the first sensing node; and

the low side circuitry comprising:

a second sensing node for connecting to the low side power device;

second sensing circuitry for providing a second sense result signal for controlling said low side driving circuit in response to a second sense input signal, the second sense input signal including information received at the second sensing node from the low side power device <u>over a second direct circuit path from said low side power device to said second sensing circuitry</u>; the second sense result signal including information derived from the second sense input signal about operation of the low side power device;

second correction circuitry <u>included in said second direct circuit path from said low side power device to said second sensing circuitry</u> for preventing the second sense input signal <u>on said second circuit path</u> from including spurious information received at the second sensing node;

said integrated circuit further comprising said high side driving circuit disposed in said integrated circuit, wherein said high side driving circuit receives an input voltage and generates a driving signal for said high side power device; and

said integrated circuit further comprising said low side driving circuit disposed in said integrated circuit, wherein said low side driving circuit receives an input voltage and generates a driving signal for said low side power device.

Claim 21 (Previously Presented)

The circuit of claim 9, in which the gating device provides spurious negative spikes, the correction circuitry preventing negative spikes in the sense input signal.

Claim 22 (Previously Presented)

The circuit of claim 17, in which the gating device provides spurious negative spikes, the correction circuitry preventing negative spikes in the sense input signal.

Claim 23 (Previously Presented)

The circuit of claim 1, wherein said spurious information includes at least one of high-frequency noise and a negative voltage spike.

Claim 24 (Currently Amended)

The circuit of claim 9, wherein said spurious information includes at least one <u>of</u> high-frequency noise and a negative voltage spike.

Claim 25 (Currently Amended)

The circuit of claim 17, wherein said spurious information includes at least one <u>of</u> high-frequency noise and a negative voltage spike.

Claim 26 (Previously Presented)

The circuit of claim 5, further comprising a driving circuit in said integrated circuit, wherein said driving circuit receives an input voltage and generates a driving signal for said power device.

Claim 27 (Previously Presented)

The circuit of claim 6, further comprising a driving circuit in said integrated circuit, wherein said driving circuit receives an input voltage and generates a driving signal for said power device.